Application No. 09/591,044
Filed: June 9, 2000
Group Art Unit: 2189

REMARKS

The instant Remarks are filed in response to the official action dated June 20, 2003. Reconsideration is respectfully requested.

Claims 1-9 are currently pending.

Claims 1-9 stand rejected.

The Examiner has rejected claims 1-4 and 6-9 under 35 U.S.C. 102(e) as being anticipated by Sotek et al. (USP 6,209,022). Specifically, regarding base claims 1 and 6, the official action indicates that the Sotek reference discloses a system for transferring data between a plurality of devices comprising a bus including a data line and a clock line, and at least one first device coupled to the bus, in which the first device is operative (1) at a first clock rate and at a second reduced clock rate, (2) to receive a portion of the data transmitted over the data line and to store the data in a register, and (3) in the event the first device is operating at the second reduced clock rate, to drive the clock line to a first predetermined level while the data is stored in the register, thereby enabling data transfer between the first device and at least one second device over the bus (see

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also column 7, lines 1-21, and column 5, lines 18-25, of Sotek et al.).

However, the Applicants respectfully submit that the Sotek reference does not teach or suggest the first device driving the *clock line* to the first predetermined logic level when operating at the reduced clock rate and while the data is stored in the register, thereby enabling data transfer between the first device and at least one second device on the bus, as recited in base claims 1 and 6. For example, page 4 of the official action indicates that the Sotek reference discloses slave stations that output bits of the first logic state "0", but when detecting that the line C/D is discharged, deactivate themselves – only those slave stations that are currently outputting a bit of the second logic state "1" remain active (see also column 5, lines 20-24, of Sotek et al.).

However, the Applicants respectfully point out that the line C/D of the Sotek system is *not* a clock line, but is instead a command and data line C/D (see column 5, lines 9-12, of Sotek et al.). The Sotek reference contains no teaching or suggestion of driving a clock line to a first predetermined logic level when

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operating at a reduced clock rate, as recited in base claims 1 and 6.

The Applicants respectfully submit that the system as claimed is fundamentally different from the system disclosed in the Sotek reference. For example, as described in the instant application, the clock line is driven to the first predetermined logic level (*e.g.*, a low logic level) to extend the low period of the clock signal, thereby enabling data transfer between devices by giving at least one of the devices additional clock cycles to complete a data read operation (see page 14, lines 17-23, and Fig. 4, of the application). In contrast, the Sotek reference discloses discharging the command and data line C/D, not the clock line. The Sotek reference further discloses pre-charging and discharging the command and data line C/D via a resistor R not for the purpose of extending the low period of a signal to enable data transfer between devices, but rather to allow parallel operation of a plurality of open-collector output circuits in a device identification operating mode (see column 7, lines 4-9, of Sotek et al.).

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Moreover, whereas the first device of base claims 1 and 6 is operative at the first clock rate and at the second reduced clock rate, *e.g.*, when executing a power management application (see page 10, lines 16-28, of the application), the lower switching speed of the Sotek system has nothing to do with implementing power management functions. Instead, Sotek et al. employ the lower switching speed simply because the plurality of open-collector output circuits included in their system cannot handle a higher switching speed - Sotek employs the higher switching speed when transferring data via a plurality of faster tri-state output circuits.

Because the Sotek reference does not describe a system that includes a first device that, in the event it is operating at a reduced clock rate, drives *a clock line* to a first predetermined logic level while data is stored in a register, thereby enabling data transfer between the first device and at least one second device over a bus, the Sotek reference does not anticipate base claims 1 and 6 and the claims dependent therefrom. Accordingly, the Applicants respectfully submit that the rejection of the claims 1-4 and 6-9 under 35 U.S.C. 102(e) is unwarranted and should be withdrawn.

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The Examiner has also rejected claim 5 under 35 U.S.C. 103(a) as being unpatentable over Sotek et al. in view of the Applicants' admitted prior art. Specifically, the official action indicates that it would have been obvious to incorporate the Applicants' admitted prior art teaching into the Sotek system for the purpose of including an SMBus in the system. However, as explained above, the Sotek reference contains no teaching or suggestion of driving a clock line to a first predetermined logic level when operating at a reduced clock rate, as recited in base claims 1 and 6. Such teaching is also nowhere to be found in the Applicants' admitted prior art. Accordingly, even if the Sotek reference and the Applicants' admitted prior art were combined as suggested, the resulting combination would not render claim 5 obvious. The Applicants therefore respectfully submit that the rejection of claim 5 under 35 U.S.C. 103(a) is unwarranted and should be withdrawn.

In view of the foregoing, it is respectfully submitted that the present application is in a condition for allowance. Early and favorable action is respectfully requested.

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The Examiner is encouraged to telephone the undersigned Attorney to discuss any matter that would expedite allowance of the present application.

Respectfully submitted,

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